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10/681,647	10/08/2003	Jung Pill Kim	2003P5259US	6096

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,647	KIM ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-7,10-13 and 15-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21,22,25 and 26* is/are allowed.

6)☒ Claim(s) *1, 5, 7, 10, 11, 13, 15-18, 23 and 24* is/are rejected.

7)☒ Claim(s) *6,12,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 10-26-04. Applicant's arguments with respect to reference Tedrow et al. (USP. 5,546,042) have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remained rejected under Tedrow.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 1, the recitation "a voltage which is generated internally to an integrated circuit device to a channel resistance of switches utilized to adjust a level of the voltage" is indefinite because it is not clear what the "a channel resistance of switches" is meant by. The recitation "providing a plurality of switches to selectively couple an **output node** on which the voltage is to be supplied, **to a single node** of the voltage dividing circuit" is misdescriptive because figure 3 of the present application shows that the switch system performs as a multiplexer. A voltage of the nodes of voltage devider (NC, ND, NE...) is coupled to the output node (NOUT) when one of the switches is energized. The voltage (Vout) is not supplied back to " a single node of the voltage dividing circuit" as recited. The same rationale is applied to claims 7 and 21.

Claims 5, 6 and 10-12 are indefinite because of the technical deficiencies of claims 1 and 7.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5, 7, 10, 11, 13, 15, 16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Tedrow et al. (US Pat. 5,546,042), the prior art of record.

Regarding claim 1, figure 2 and 5 of Tedrow show a method for reducing a sensitivity of a voltage which is generated internally to an integrated circuit device to a channel resistance of switches utilized to adjust a level of the voltage, the method comrising:

providing a voltage dividing circuit with a plurality of serially connected resisors (R3-Rk);

supplying the voltage dividing circuit with a reference voltage (Vref) , resulting in a different voltage level at nodes of the voltage dividing circuit formed between the serially connected resistors;

providing a plurality of switches (N2-Nk), to selectively couple an output node (Vout).

providing control signals to close a single one of the switches at any given time, wherein each of the control signals corresponds to a different one of the switches; and only one of the control signals is asserted at any time to close a single switch; and

generating the control signals from one or more non-volatile-storage elements (col. 3 lines 37-43; col. 4, lines 34-56).

Regarding claims 5, the control signals for switches (N2-Nk) are generated by a single element of the circuit: the "a control engine" (col. 7, lines 35-38).

Regarding claim 7, figure 2 and 5 of Tedrow show trimming circuit for use in adjusting a voltage generated internally to an integrated circuit device, comprising: a plurality of switches (N2-Nk) to selectively couple the voltage at a single one of a plurality of nodes of a voltage dividing circuit (divider (R3-Rk) to the output node, each node is at a different voltage level. The switches are coupled between the output node and each node of the voltage dividing circuit. The switches are opened or closed

in response to the signal generated by non-volatile-storage elements (col. 3 lines 37-43; col. 4, lines 34-56).

Regarding claim 10, figure 3 of Tedrow shows the detail of the non-volatile memory device (30). The decoder (54) decodes data from memory array 50 (non-volatile) for generating control signals (col. 3, lines 37-45; col. 4, lines 27-46; col.7, lines 35-39).

Regarding claim 11, the number of switches (N2-Nk) is greater than the number of non-volatile storage elements (50).

Regarding claim 13, figures 2 and 5 of Tedrow shows a memory device comprising: peripheral circuitry (39); a plurality of memory cells in circuit (30); a voltage generating circuit comprising a voltage divider circuit (R3-Rk) with a plurality of nodes, each at different voltage levels dependent on a reference voltage, and a plurality of switches (N2-Nk) to selectively couple an output node (Vout) of the voltage generating circuit with a single one of the voltage divider circuit nodes. The switches are coupled between the output node and each node of the voltage dividing circuit. The switches are opened or closed in response to the signal generated by non-volatile-storage elements (col. 3 lines 37-43; col. 4, lines 34-56).

Regarding claim 15, the non-volatile memory element (30) generates signals for controlling the switches. The decoder is element (54) in figure 3.

Regarding claim 16, it is inherent that a negative voltage can be generated when (Vpp) is a negative voltage source.

Regarding claim 18, the voltage regulation circuit, figure 5, provides a high precision programming voltage for programming memory cells (abstract). Inherently, it provide voltage to the wordlines of the memory cells.

Claim Rejections - 35 USC § 103

Claims 17, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tedrow et al. (US Pat. 5,546,042) in view of Hoenigschmid et al. (US Pat. 5,970,009).

Regarding claim 17, figures 2 and 5 of Tedrow include all the limitation of claim 17 except for the limitation that the voltage generating circuit is configured to generate a negative voltage and the memory device is a dynamic RAM. However, it is well known and it is obvious that when the voltage applied to the voltage divider is negative with respect to the ground, the voltage divider generates negative output voltages. Figures 2 and 5 of Tedrow show that the memory device is a nonvolatile device. Figures 2 and 5 of Tedrow do not show that the memory device can be a dynamic random access device having a negative voltage applied to the substrate of the transistors of the memory cell. However, it is old and well known that with the memory comprising DRAM, the stored data in the DRAM can be changed according to the requirement of the application and a negative voltage is applied to the substrate of the memory cell transistor for reducing substrate sensitivity and diffusion capacitance (US Pat. 5,970,009, col. 1, lines 39-44). Therefore, it would have been obvious to those skilled in the art to replace the nonvolatile memory device of Tedrow with the DRAM device having a negative voltage applied to the substrate of the transistors of the memory cell for changing the data according to the requirement of the application and for reducing substrate sensitivity and diffusion capacitance.

Regarding claims 23 and 24, figures 2, 3 and 5 of Tedrow show a memory device comprising: peripheral circuitry (50, 52, 54, 65, 58, 60, 62, 64); plurality of memory cells (50); a voltage generating circuit (45). Figure 5 of Tedrow does not show that the voltage generating can output a negative voltage. However, it is well known in the art and would have been obvious that when a negative voltage is applied to the voltage divider, it will generate negative voltages. Figures 2, 3 and 5 of Tedrow do not show that the memory device can be a dynamic random access device having a negative voltage applied to the substrate of the transistors of the memory cell. However, it is old and well known that with the memory comprising DRAM, the stored data in the DRAM can be changed according to the requirement of the application and a negative voltage is applied to the substrate of the memory cell transistor for reducing substrate sensitivity and diffusion capacitance (US Pat. 5,970,009, col. 1, lines 39-44). Therefore, it would have been obvious to those skilled

in the art to replace the nonvolatile memory device of Tedrow with the DRAM device having a negative voltage applied to the substrate of the transistors of the memory cell for changing the data according to the requirement of the application and for reducing substrate sensitivity and diffusion capacitance. The voltage regulation circuit, figure 5, provides a high precision programming voltage for programming memory cells (abstract). Inherently, it provides voltage to the wordlines of the memory cells.

Allowable Subject Matter

Claims 19 and 20 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6 and 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 21, 22, 25 and 26 are allowed.

Claims 6, 12 would be allowable because the prior art (USP. 5,546,042) fails to teach or suggest one or more switches in parallel with one or more of the resistors of the voltage dividing circuit, each to selectively bypass the one or more resistors.

Claims 19 and 20 are objected to because the prior art (USP. 5,546,042) fails to teach or suggest a memory device comprising a voltage dividing circuit having one or more switches in parallel with one or more of the resistors of the voltage dividing circuit, each to selectively bypass the one or more resistors as called for in claim 19; a plurality of fuses for generating control signals for the switches as called for in claim 20.

Claims 21, 22, 25 and 26 are allowed because the prior art (USP. 5,546,042) fails to teach or suggest a method for reducing a sensitivity of a voltage, the method comprising providing one or more switches in parallel with one or more of the resistors of the voltage dividing circuit, each to selectively bypass the one or more resistors as called for in claims 21, 22, 25; a plurality of fuses for generating control signals for the switches as called for in claim 26.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

12-29-04

TUAN T. LAM
PRIMARY EXAMINER